Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claim 1 (previously amended): An apparatus comprising:

an input block to apply an input signal to a common input terminal of a sensing block; and

a converting block to receive a sensed signal from a sensing block in response to the input signal.

Claim 2 (previously amended): The apparatus of claim 1, wherein the converting block is coupled to provide an output signal based on the sensed signal.

Claim 3 (previously amended): The apparatus of claim 1, wherein the converting block is coupled to provide a signal having a fractional pulse density that is indicative of acceleration.

Claim 4 (previously amended): The apparatus of claim 1, wherein the input block is coupled to apply a first signal to the common input terminal during a first clock phase and a second signal during a second clock phase.

Claim 5 (previously amended): The apparatus of claim 1, wherein the converting block is configured to integrate the sensed signal and provide a first output signal and a second output signal.

Claim 6 (previously amended): The apparatus of claim 5, wherein the converting block is further configured to compare the first output signal and the second output signal and provide an output signal.

Claim 7 (previously amended): The apparatus of claim 6, wherein the converting block is coupled to provide the output signal to the input block.

Claim 8 (previously amended): The apparatus of claim 1, wherein the input block comprises a first input capacitor and a second input capacitor, wherein the input block is coupled to provide a first input signal to the converting block through the first input capacitor and a second input signal to the converting block through the second input capacitor.

Claim 9 (previously amended): The apparatus of claim 8, wherein the input block is coupled to provide the first input signal through the first capacitor and the second input signal through the second capacitor.

Claim 10 (original): The apparatus of claim 1, further comprising a storage unit to store one or more voltage values to apply to the apparatus.

Claim 11 (currently amended): A method comprising:

providing [an input] a first signal to a common input terminal of a sensing block during a first clock phase and a second signal to the common input terminal during a second clock phase, wherein the first clock phase and the second clock phase have non-overlapping clock cycles;

receiving a sensed signal from the sensing block based on providing the [input] first signal and the second signal; and

providing a signal based on the sensed signal.

Claim 12 (original): The method of claim 11, comprising providing a digital signal based on the sensed signal.

Claim 13 (currently amended): The method of claim 11, comprising providing the signal having a fractional pulse density that is indicative of acceleration.

Claim 14 (canceled)

Claim 15 (canceled)

Claim 16 (currently amended): The method of claim [15] 11, comprising integrating the sensed signal and providing a first output signal and a second output signal.

Claim 17 (currently amended): The method of claim 16, comprising comparing the first output signal and the second output signal and [provides] providing an output signal.

Claim 18 (original): The method of claim 17, comprising providing the first signal and second signal based at least in part on the output signal.

Claim 19 (original): An apparatus, comprising:

an input block to provide an input signal to a common terminal of a first capacitor and a second capacitor of a sensing block; and

a converting block to receive a sensed signal from the sensing block in response to applying the input signal.

Claim 20 (previously amended): The apparatus of claim 19, wherein the converting block is coupled to provide a digital signal based on the sensed signal.

Claim 21 (previously amended): The apparatus of claim 19, wherein the input block is coupled to apply a first signal to the common input terminal during a first clock phase and a second signal during a second clock phase.

Claim 22 (previously amended): The apparatus of claim 19, wherein the input block comprises a first input capacitor and a second input capacitor, wherein the input block is coupled to provide a first input signal to the converting block through the first input capacitor and a second input signal to the converting block through the second input capacitor.

Claim 23 (original): The apparatus of claim 19, wherein the converting block comprises:

an integrator to receive the sensed signal from the sensing block and to produce an integrated signal;

a comparator to receive the integrated signal and to provide an output signal; and

a latch to receive the output signal and to provide a latched output signal.

Claim 24 (original): The apparatus of claim 19, further comprising a storage unit to store one or more voltage values to apply to the sensing circuit.

Claim 25 (original): A restraint system, comprising:

a sensing circuit to:

apply an input signal to a common input terminal of a sensing block;

receive a sensed signal from the sensing block in response to applying the input signal; and

provide an output signal based at least in part on the sensed signal; and

a deployment block to provide an activation signal based at least in part on the output signal from the sensing circuit.

Claim 26 (previously amended): The restraint system of claim 25, wherein the deployment block is coupled to provide the activation signal to activate an airbag.

Claim 27 (previously amended): The restraint system of claim 25, wherein the sensing circuit is coupled to be clocked via a plurality of non-overlapping clocks.

Claim 28 (previously amended): The restraint system of claim 25, wherein the sensing circuit is configured to provide a digital signal.

Claim 29 (previously amended): The restraint system of claim 25, wherein the sensing circuit is coupled to provide a signal having a fractional pulse density that is indicative of acceleration.

Claim 30 (original): The restraint system of claim 25, further comprising a storage unit to store one or more voltage values to apply to the sensing circuit.